REMARKS

In the Office Action of March 27, 2006, the Examiner (1) objected to claims 1, 2, 9 and 10 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,606,743 ("Raz"); 2) rejected claims 11, 12, 3 and 4 under 35 U.S.C. § 103(a) 35 U.S.C. § 102 as obvious over Raz in view of U.S. Patent No. 6,748,495 ("Rowlands"); 3) rejected claims 13 and 5 as obvious over Raz in view of Rowlands and further in view of U.S. Patent No. 5,699,551 ("Taylor"); 4) rejected claims 14-15, and 6-7 as obvious over Raz in view of U.S. Patent No. 5,479,636 ("Vanka et al"); 5) rejected claims 16 and 8 as obvious over Raz in view of Vanka and further in view of Taylor. Applicants traverse the claim rejections, based for the reasons provided below, and submit new claims 17 and 18.

Applicants have amended the specification to include serial numbers of various referenced pending applications.

Without limiting the scope of the claims in anyway, Applicants offer the following comments to assist the Examiner in examining this case. Applicants' contribution relates to the fact that only the top of a stack is ever accessed (either via push or pop operation) from the stack. Each time the top of the stack is read, the top of stack pointer moves down to point the next value (which is now the top of the stack). A stack-based data structure can be stored in cache memory. Thus, if a stack is stored in cache and the top of the stack coincides with, for example, the last word in the line, the remaining words in the line (representing the data that were previously at the top of the stack) are no longer valid data for the stack. Thus, when the top of the stack happens to coincide to the last word in the line and is popped off the stack, the entire cache line can be invalidated thereby offering the line for replacement by new data. Invalidating the entire cache line that does not contain stack data would normally not be permissible merely by removing a terminal word from the cache line.

Claim 1 requires "varying the memory management policies depending on whether the data being removed corresponds to a predetermined word in the cache line." The Examiner referred to Raz, col. 4, lines 19-36, for this limitation:

> The smart DMA controller 14 is configured to read and write the content of the entire intelligent stack 12 to or from the memory 30, such as when it is

> required to shift between different tasks. The smart DMA controller 14 also corrects potential stack overflow or underflow by temporarily storing any excess of data from the intelligent stack 12 to the memory 30. The smart DMA will dump a block of words to main memory 30 when the stack approaches overflow (on Push operation), or will load a block of words from main memory 30 when the stack approaches underflow (on Pop operation). The smart DMA controller can load a local variable from main memory 30 (on Variable Load miss), store a local variable to main memory 30 (on Variable Store miss), dump the entire cache 38 to main memory 30 to prepare for a context switch, or load the entire cache 38 from memory 30 to perform a context switch. The smart DMA can also optionally be used to accelerate thread context switching by moving data into and out of the cache 38, as required.
>
> It should be noted that the inventive program language accelerator 10 could be made to operate without the smart DMA controller 14, although the addition of the smart DMA controller 14 does significantly increase the usefulness and functionality of the program language accelerator 10.

The above-quoted passage from Raz does not teach or even suggest that the memory management policy can or should be varied based on whether data to be removed from a cache is from a particular predetermined word within the cache line. No other art of record satisfies this deficiency of Raz. For least this reason, claim 1 and its dependent claims are patentable.

The same or similar reason articulated above with regard to claim 1 also applies to claim 9. Accordingly, claim 9 and its dependent claims are in condition for allowance as well.

New independent claim 17 requires that "the controller invalidates an entire line of said cache memory upon the processor reading a value from the top of the stack if said value from the top of the stack comprises a word at a predetermined location with said line." None of the art of record teaches or suggests this limitation.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including

fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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